Experiment 6: Introduction to Flip-Flops
Every student has to prepare a preliminary work and also he/she should simulate the circuit, designed for the experimental work - by using a simulation program, such as Logisim.

SEQUENTIAL CIRCUIT

Logic circuits for digital systems can generally be classified into two categories: combinational logic circuit and sequential logic circuit. A sequential circuit consists of a combinational circuit to which memory elements are connected to, in order to form a feedback path. The sequential circuit receives binary information from external inputs and - together with the present states of memory elements - determine the output and the next state of memory elements.

There are two main types of sequential circuits whose behaviour depend on the timing of their signals. A *Synchronous sequential circuit* is a system whose behavior can be defined from the knowledge of its signals at discrete instants of time. Synchronization is achieved by timing device, which generates a periodic train of clock pulses. Synchronous sequential circuits that use clock pulses in the inputs of memory elements are called clocked sequential circuit. Flip-flops are circuits that can maintain their state indefinitely as long as power is supplied, and change their states when directed to by a control input. Flip-flops are given a *clock* input, which specifies specific moments in time to change state. What makes flip-flops special is that their output is connected back into their input, so that their proceeding state depends on both their current state and their control input. Thus, when analyzing a flip-flop, we look at its inputs and its current output, or *state* (usually labeled Q(t)), and from those, determine its next state (usually labeled Q(t+1)). The *Asynchronous sequential circuits* do not use clock pulses. The change of internal state occurs when there is a change in the input variables. The memory elements in asynchronous sequential circuits are either unclocked flip-flops or time delay elements. The design of asynchronous sequential circuits is more difficult than synchronous sequential circuits because of the timing problems involved in the feedback.
Main elements of controlled latch circuits:

**D Latch**

Characteristic equation $Q(t+1) = D$

![D Latch Circuit Diagram]

**Operation of a D Latch:**

**Case 1:**

$\text{Clock} = 0$

$x = y = 1, w = Q'(t), z = Q(t)$

$Q(t+1) = z \cdot w = Q(t)$

$Q'(t+1) = y \cdot z = Q'(t)$

**Case 2:**

$\text{Clock} = 1, D = 0, Q(t) = 0$ and $Q'(t) = 1$

$x = \overline{D} = 1, y = D = 0$

$Q(t+1) = 0$ and $Q'(t+1) = 1$

**Case 3:**

$\text{Clock} = 1, D = 0, Q(t) = 1$ and $Q'(t) = 0$

$x = \overline{D} = 1, y = D = 0$

Before reaching the stable state, there is a transition state $Q_t$ such that

$Q_t = Q'_t = 1$ (therefore $w = z = 1$)

Then the stable state is reached such that:

$Q(t+1) = 0$ and $Q'(t+1) = 1$

**Case 4:**

$\text{Clock} = 1, D = 1, Q(t) = 0$ and $Q'(t) = 1$

$x = 0, y = 1$

Before reaching the stable state, there is a transition state $Q_t$ such that

$Q_t = Q'_t = 1$ (where $w = z = 1$)

Then the stable state is reached:

$Q(t+1) = 1$ and $Q'(t+1) = 0$

**Case 5:**

$\text{Clock} = 1, D = 1, Q(t) = 1$ and $Q'(t) = 0$

$x = 0, y = 1$

$Q(t+1) = 1$ and $Q'(t+1) = 0$
RS Latch

Characteristic equation $Q(t+1) = S\cdot R \cdot Q(t)$

The latch circuits given above change state only when a clock signal is present. However, the clock signal is not necessarily instantaneous, so there needs to be a way to prevent the circuit from changing state multiple times during a clock cycle. There are 2 ways to achieve this. One is to only change state once the clock cycle is finished. This type of circuit is called a master-slave flip-flop. The other is a flip-flop that only triggers during a signal transition. This type is called an edge-triggered flip-flop.
Master-Slave Flip-Flop

The master-slave flip-flop works by allowing one flip-flop to change state as the clock pulse is active. The output from that flip-flop goes into another flip-flop, which is attached to an inverted clock input. Thus, the state of the first flip-flop will have settled by the time its output changes the state of the second flip-flop after the clock pulse has finished, and stable output will have been achieved.

![Diagram of Master-Slave Flip-Flop](image)

**Figure 2**: RS master-slave flip flop

![Timing Diagram](image)

**Figure 3**: A timing diagram for the RS master-slave flip flop in Figure 2.
Figures 2 and 3 show an RS master-slave flip flop (composed of two RS latches) and its timing diagram, respectively. When the clock is at logic 1, the data at R and S inputs are transferred into the master while when the clock is at logic 0, the master is isolated from the input data and the state of the master is transferred to the slave.

In Figure 3, at the triggering edges A, B, C the state of master is transferred to the slave.

At point A, \( S = 0, R = 1 \). Since \( S2 = Q1 = 0 \) and \( R2 = Q1' = 1 \), \( Q = 0 \).

At point B, \( S = 1, R = 0 \). \( S2 = Q1 = 1 \). \( R2 = Q1' = 0 \) and output becomes \( Q = 1 \).

At point C, \( S = 0, R = 1 \). \( S2 = Q1 = 0 \) and \( R2 = Q1' = 1 \), therefore \( Q = 0 \).

**Edge-Triggered Flip-Flop**

Another type of flip-flop that synchronizes the state changes during a pulse transition is edge-triggered flip-flops. Edge triggered flip-flops trigger only when the pulse is in transition. Some trigger during a positive transition (going from 0-to-1), and are called **positive edge triggered flip-flops**. Others trigger during a negative transition (going from 1-to-0), and are called **negative edge triggered flip-flops**.

![Diagram of a positive edge triggered D flip-flop](image)

**Figure 4**: A timing diagram for a positive edge triggered D flip flop
Preliminary Work:

1) What is the difference between master-slave FF and edge triggered FF?

2) In the figure below there is an X FF. Find the characteristic table of the FF. What kind of a Flip-Flop is this?

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Experimental Work:

1) Implement the X FlipFlop designed in your preliminary work and analyze the circuit.

2) Construct the circuit shown in figure by using D FF’s:
Pin Connections:

<table>
<thead>
<tr>
<th>4013 - Dual D-type Flip-flop</th>
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<tbody>
<tr>
<td>Pins 4, 6, 7, 8, 10 = Ground</td>
</tr>
<tr>
<td>Pin 14 (Vdd) = + 5 Vdc</td>
</tr>
<tr>
<td>Pin 5 (D1) = D input of FF1</td>
</tr>
<tr>
<td>Pin 1 (O1) = Output of FF1</td>
</tr>
<tr>
<td>Pin 3 (CP1) = Clock pulse of FF1</td>
</tr>
<tr>
<td>Pin 9 (D2) = D input of FF2</td>
</tr>
<tr>
<td>Pin 13 (O2) = Output of FF2</td>
</tr>
<tr>
<td>Pin 11 (CP2) = Clock pulse of FF2</td>
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